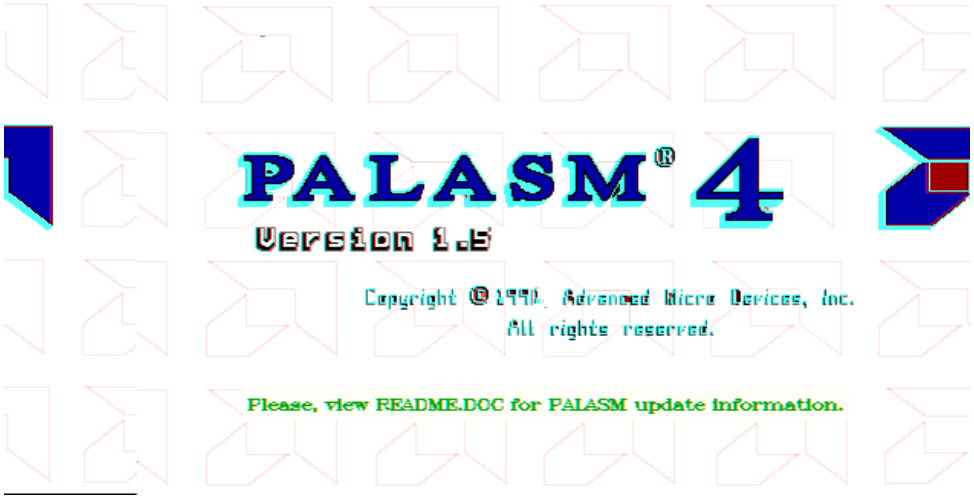
Lab-Report

Digital Electronics

Use of Palasm Software



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Group: A
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Date: 02/11/1998

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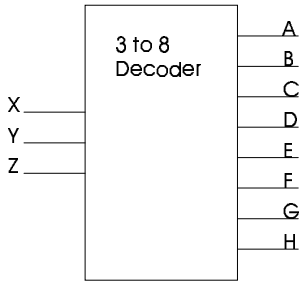
Contents

1. Familiarisation

Palasm is an AMD software package for programming and simulation digital electronic circuits like PALs, GALs, etc.. It generates Standard JEDEC codes.
At the first stage of the lab an example file was to be accessed and simulated.
The following example file “Tutor1.PDS” is an 8 to 3 decoder, which codes the three inputs X, Y ,Z into 8 outputs named A – H. Therefore a PAL16L8 is used.

1.1 Schematic of an 8 to 3 decoder



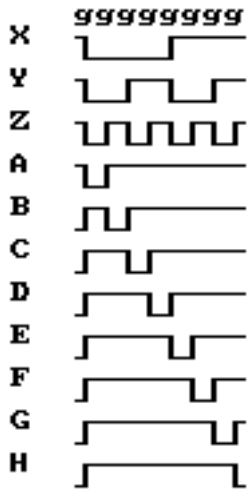
1.2 PALASM listing of a 3 to 8 line decoder (example file):

```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
˝
TITLE    TUTOR1.PDS
˝
PATTERN A
˝
REVISION 1.0
˝
AUTHOR   J.ENGINEER
˝
COMPANY  ADVANCED MICRO DEVICES
˝
DATE     01/01/90

CHIP  DECODER  PAL16L8

;---------------------------------- PIN Declarations ---------------
PIN  2          X                    COMBINATORIAL             ; INPUT
PIN  3          Y                    COMBINATORIAL             ; INPUT
PIN  4          Z                    COMBINATORIAL             ; INPUT
PIN  10         GND                                            ; INPUT
PIN  12         A                    COMBINATORIAL             ; OUTPUT
PIN  13         B                    COMBINATORIAL             ; OUTPUT
PIN  14         C                    COMBINATORIAL             ; OUTPUT
PIN  15         D                    COMBINATORIAL             ; OUTPUT
PIN  16         E                    COMBINATORIAL             ; OUTPUT
PIN   17        F                    COMBINATORIAL             ; OUTPUT
PIN  18         G                    COMBINATORIAL             ; OUTPUT
PIN  19         H                    COMBINATORIAL             ; OUTPUT
PIN  20         VCC                                            ; INPUT
```

```
;---------------------------------- Boolean Equation Segment ------
EQUATIONS
/A = /X * /Y * /Z
/B = /X * /Y *  Z
/C = /X *  Y * /Z
/D = /X *  Y *  Z
/E =  X * /Y * /Z
/F =  X * /Y *  Z
/G =  X *  Y * /Z
/H =  X *  Y *  Z


;---------------------------------- Simulation Segment ------------
˝
SIMULATION
˝
TRACE_ON X Y Z A B C D E F G H
˝
SETF  /X /Y /Z
˝
CHECK /A  B  C  D  E  F  G  H
˝
SETF  /X /Y  Z
˝
CHECK  A /B  C  D  E  F  G  H
˝
SETF  /X  Y /Z
˝
CHECK  A  B /C  D  E  F  G  H
SETF  /X  Y  Z
CHECK  A  B  C /D  E  F  G  H
SETF   X /Y /Z
CHECK  A  B  C  D /E  F  G  H
SETF   X /Y  Z
CHECK  A  B  C  D  E /F  G  H
SETF   X  Y /Z
CHECK  A  B  C  D  E  F /G  H
SETF   X  Y  Z
CHECK  A  B  C  D  E  F  G /H
TRACE_OFF

;-------------------------------------------------------------------
•
```

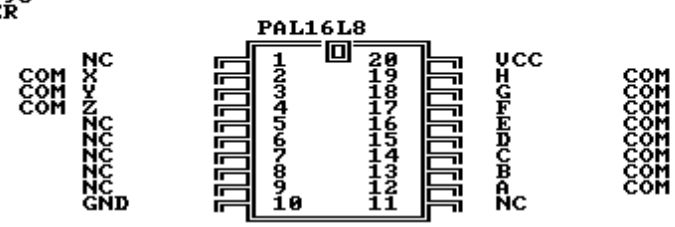
The declaration segment is used for project information, like manufacturer, developing engineer, date, etc..
In the following Pin Declaration part of the listing the Pins of the PAL are initialised.
The 3rd Part of the listing now shows the boolean expressions for the 3 to 8 line decoder.
In the simulation segment the circuit can be checked whether the output are working exactly like they should do.
So the input X, Y, Z are set by the SETF function (a slash in front of a variable stands for a negation) and the outputs are checked by means of the CHECK function.
The simulation can be viewed as waveform in order to obtain easily checkable results.
If the outputs are not on the expected levels an error is shown in the circuit simulation.
The simulation starts with the TRACE_ON <variables> and ends with the TRACE_OFF command.

1.3 Output waveform obtained from simulation:



1.4 Also a pinout of the design file can be viewed and printed:

```
TITLE:      TUTOR1.PDS
PATTERN:    A
REVISION:   1.0
AUTHOR:     J.ENGINEER
COMPANY:    ADVANCED MICRO DEVICES
DATE:       01/01/90
MACRO:      DECODER
```



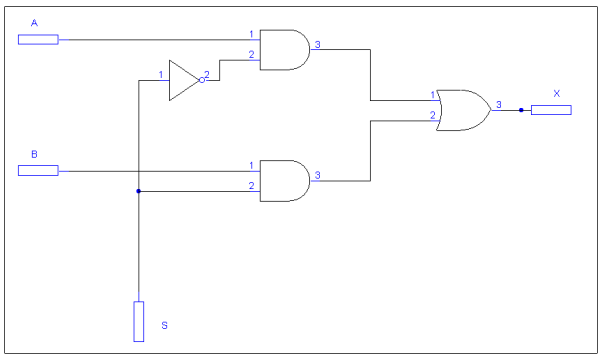
The pinout is directly derived from the declaration segment in the listing and every change in the listing appears in the pinout view.

2. Combinatorial Logic Design

A simple logic circuit was to be designed and implemented with a PAL16L8. The simulation was to be carried out for checking the design on correct function.

2.1 Truth table and schematic of a 2 to 1 multiplexer

A	**B**	**S**	**X**
0	0	0	**0**
0	0	1	**0**
0	1	0	**0**
0	1	1	**1**
1	0	0	**1**
1	0	1	**0**
1	1	0	**1**
1	1	1	**1**



2.2 Boolean Equation of a 2 to 1 mux

$$Q = \left(A \cdot \bar{S}\right) + \left(B \cdot S\right)$$

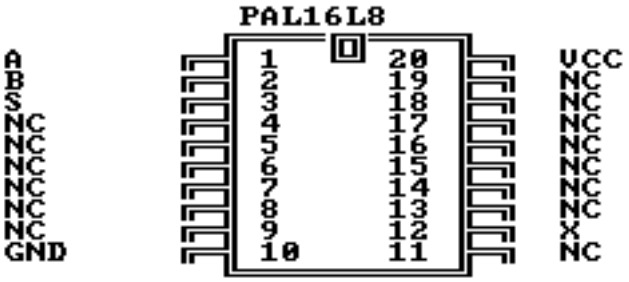
This equation was to derive from the truth table and the implementation with PALASM is shown in the listing on the following page.

```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE    2to1 Multiplexer
PATTERN
REVISION
AUTHOR
COMPANY
DATE     10/07/98

CHIP  _mux21  PAL16L8

;---------------------------------- PIN Declarations ---------------
PIN  1          A                                                  ; INPUT
PIN  2          B                                                  ; INPUT
PIN  3          S                                                  ; INPUT
PIN  12         X                                                  ; OUTPUT

;---------------------------------- Boolean Equation Segment ------
EQUATIONS
X=A*/S+B*S
;---------------------------------- Simulation Segment ------------
SIMULATION
TRACE_ON A B S X
SETF /A /B /S
CHECK /X
SETF /A /B  S
CHECK /X
SETF /A  B /S
CHECK /X
SETF /A  B  S
CHECK  X
SETF  A /B /S
CHECK  X
SETF  A /B  S
CHECK /X
SETF  A  B /S
CHECK  X
SETF  A  B  S
CHECK  X
TRACE_OFF
;-------------------------------------------------------------------
•
```

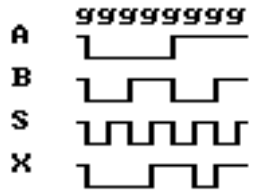
2.3 Pinout print of PALASM

The pinout print is automatically generated by palasm and can be saved into a file or directly printed out.

```
TITLE:      2to1 Multiplexer
PATTERN:
REVISION:
AUTHOR:
COMPANY:
DATE:       10/07/98
MACRO:      _MUX21
```



2.4 Waveform simulation of Mux 21

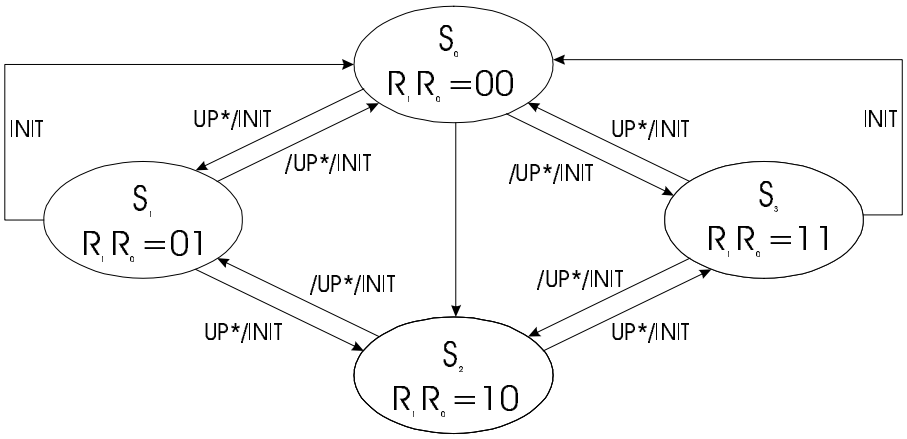


The waveform correspondents to the expected values.

3. Sequential logic design → 2-Bit Up/Down Counter

A 2-Bit Up/Down Counter is to be implemented and simulated with a PAL16V8. The counter is realised by means of the state machine of PALASM.

3.1 State diagram of the 2-Bit up/down counter



3.2 Listing of the 2-Bit up/down counter

The following listing shows the realisation and simulation of the 2-Bit up/down counter realised with PALASM.

```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE    2-BIT UP/DOWN COUNTER
PATTERN
REVISION 0.01
AUTHOR   DIRK BECKER, BENG, GROUP A
COMPANY  UEL
DATE     10/07/98, 27/10/98

CHIP  _2BITCNT  PALCE16V8

;---------------------------------- PIN Declarations ---------------
PIN  1          CLK                                              ;
PIN  2          UP                                               ;
PIN  3          INIT                                             ;
PIN  11         OE                                               ;
PIN  15         R1                                  REGISTERED ;
PIN  14         R0                                  REGISTERED ;

;---------------------------------- State Machine Equations ------
STATE
MOORE_MACHINE
DEFAULT_BRANCH S0

;State Assignments
;State are the same as the output

S0=/R1*/R0  ; COUNT 0
S1=/R1* R0  ; COUNT 1
S2= R1*/R0  ; COUNT 2
S3= R1* R0  ; COUNT 3

;STATE AND TRANSITION  DEFINITIONS

S0:=COUNT_UP -> S1 + COUNT_DOWN -> S3
S1:=COUNT_UP -> S2 + COUNT_DOWN -> S0
S2:=COUNT_UP -> S3 + COUNT_DOWN -> S1
S3:=COUNT_UP -> S0 + COUNT_DOWN -> S2

CONDITIONS

COUNT_UP=   UP*/INIT
COUNT_DOWN=/UP*/INIT
```

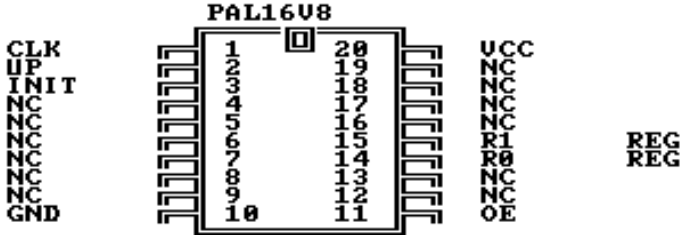
```
;---------------------------------- Simulation Segment ------------
SIMULATION

TRACE_ON INIT UP OE CLK R0 R1
SETF /INIT /OE UP /clk
FOR I:= 1 TO 4 DO    ; standard up-counting
   BEGIN
      CLOCKF clk
      clockf /clk
   END
SETF /INIT /OE /UP /CLK  ; standard down-counting
FOR I:= 1 TO 4 DO
  BEGIN
      CLOCKF CLK
      CLOCKF /CLK
  END
SETF INIT /OE /UP /CLK   ; initialisation
FOR I:= 1 TO 4 DO
   BEGIN
      CLOCKF CLK
      CLOCKF /CLK
   END
SETF /INIT OE /UP /CLK ; outputs disabled
FOR I:= 1 TO 4 DO
   BEGIN
      CLOCKF CLK
      CLOCKF /CLK
   END

TRACE_OFF


;-------------------------------------------------------------------
```

•

In the “Declaration Segment” the general circuit tasks are given and the pins are assigned like in the listings of the decoder and the multiplexer.
The differences are beginning at the second part, the “State Machine”. The state machine describes the transition from one state to the next state via the clock function. Every next clock the state machine changes to the next condition.
By use of the state machine the outputs are depending on state

3.3 Pinout of the 2-Bit up/down counter

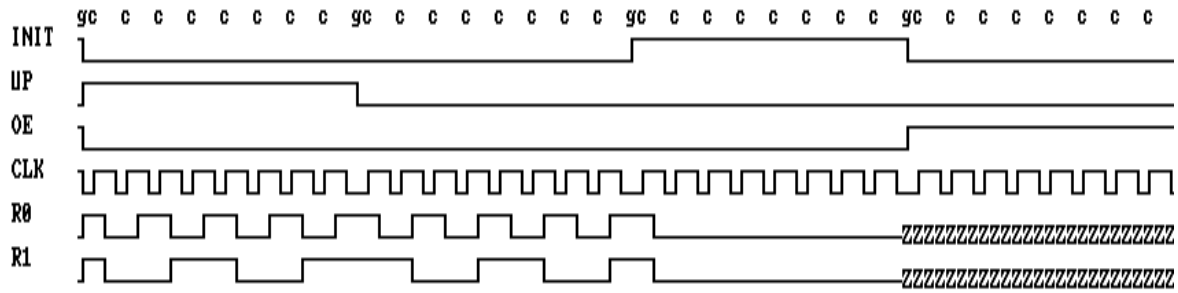
```
TITLE:      2-BIT UP/DOWN COUNTER
PATTERN:
REVISION:   0.01
AUTHOR:     DIRK BECKER, BENG, GROUP A
COMPANY:    UEL
DATE:       10/07/98, 27/10/98
MACRO:      _2BITCNT
```



3.4 Truth table of the 2-Bit up/down counter

/OE	UP	INIT	Operation
0	1	0	**Count up**
0	0	0	**Count down**
0	X	X	**Initialising**
1	X	X	**Disabled**

3.5 Simulation of the 2-Bit up/down counter



A comparision between the truth table and the waveform shows the correct working of the counter. An automatic check of the software was here not programmed, because it would be very complex, and errors can occur very easily.

3.6. Diassembler

Palasm writes JEDEC files. The JEDEC files contain the information about the programming (fuse blowing) of the used integrated circuit (IC, here PAL). In the JEDEC files are no comments or formatting options stored. By means of the diassembler a Palasm simulation file can be restored from any existing JEDEC file.
The binary data containing JEDEC file of the 2-Bit counter is shown in the following listing:

```
PALASM4  PAL ASSEMBLER   - MARKET RELEASE 1.5a (8-20-92)
 (C) - COPYRIGHT ADVANCED MICRO DEVICES INC., 1992


TITLE   :2-BIT UP/DOWN COUNTER    AUTHOR :DIRK BECKER, BENG, GROUP A
PATTERN :                         COMPANY:UEL
REVISION:0.01                     DATE   :10/07/98, 27/10/98

^
PAL16V8
_2BITCNT*
QV0036*
QP20*
QF2194*
G0*F0*
L0000 00000000000000000000000000000000*
L0032 00000000000000000000000000000000*
L0064 00000000000000000000000000000000*
L0096 00000000000000000000000000000000*
L0128 00000000000000000000000000000000*
L0160 00000000000000000000000000000000*
L0192 00000000000000000000000000000000*
L0224 00000000000000000000000000000000*
L0256 00000000000000000000000000000000*
```

```
L0288 00000000000000000000000000000000*
L0320 00000000000000000000000000000000*
L0352 00000000000000000000000000000000*
L0384 00000000000000000000000000000000*
L0416 00000000000000000000000000000000*
L0448 00000000000000000000000000000000*
L0480 00000000000000000000000000000000*
L0512 00000000000000000000000000000000*
L0544 00000000000000000000000000000000*
L0576 00000000000000000000000000000000*
L0608 00000000000000000000000000000000*
L0640 00000000000000000000000000000000*
L0672 00000000000000000000000000000000*
L0704 00000000000000000000000000000000*
L0736 00000000000000000000000000000000*
L0768 00000000000000000000000000000000*
L0800 00000000000000000000000000000000*
L0832 00000000000000000000000000000000*
L0864 00000000000000000000000000000000*
L0896 00000000000000000000000000000000*
L0928 00000000000000000000000000000000*
L0960 00000000000000000000000000000000*
L0992 00000000000000000000000000000000*
L1024 10111011111111111101110111111111*
L1056 01111011111111111110110111111111*
L1088 01111011111111111101111011111111*
L1120 10111011111111111110111011111111*
L1152 00000000000000000000000000000000*
L1184 00000000000000000000000000000000*
L1216 00000000000000000000000000000000*
L1248 00000000000000000000000000000000*
L1280 11111011111111111111111011111111*
L1312 00000000000000000000000000000000*
L1344 00000000000000000000000000000000*
L1376 00000000000000000000000000000000*
L1408 00000000000000000000000000000000*
L1440 00000000000000000000000000000000*
L1472 00000000000000000000000000000000*
L1504 00000000000000000000000000000000*
L1536 00000000000000000000000000000000*
L1568 00000000000000000000000000000000*
L1600 00000000000000000000000000000000*
L1632 00000000000000000000000000000000*
L1664 00000000000000000000000000000000*
L1696 00000000000000000000000000000000*
L1728 00000000000000000000000000000000*
L1760 00000000000000000000000000000000*
L1792 00000000000000000000000000000000*
L1824 00000000000000000000000000000000*
L1856 00000000000000000000000000000000*
L1888 00000000000000000000000000000000*
L1920 00000000000000000000000000000000*
L1952 00000000000000000000000000000000*
L1984 00000000000000000000000000000000*
L2016 00000000000000000000000000000000*
L2048 11111111000000000000000000000000*
L2080 00000000000000000000000000000000*
L2112 00000000111100111111111111111111*
L2144 11111111111111111111111111111111*
L2176 11111111111111101*
X0*
V0001 010XXXXXXN0XXHHXXXXN*
V0002 C10XXXXXXN0XXLLXXXXN*
```

```
V0003 C10XXXXXXN0XXHLXXXXN*
V0004 C10XXXXXXN0XXLHXXXXN*
V0005 C10XXXXXXN0XXHHXXXXN*
V0006 C10XXXXXXN0XXLLXXXXN*
V0007 C10XXXXXXN0XXHLXXXXN*
V0008 C10XXXXXXN0XXLHXXXXN*
V0009 C10XXXXXXN0XXHHXXXXN*
V0010 000XXXXXXN0XXHHXXXXN*
V0011 C00XXXXXXN0XXLHXXXXN*
V0012 C00XXXXXXN0XXHLXXXXN*
V0013 C00XXXXXXN0XXLLXXXXN*
V0014 C00XXXXXXN0XXHHXXXXN*
V0015 C00XXXXXXN0XXLHXXXXN*
V0016 C00XXXXXXN0XXHLXXXXN*
V0017 C00XXXXXXN0XXLLXXXXN*
V0018 C00XXXXXXN0XXHHXXXXN*
V0019 001XXXXXXN0XXHHXXXXN*
V0020 C01XXXXXXN0XXLLXXXXN*
V0021 C01XXXXXXN0XXLLXXXXN*
V0022 C01XXXXXXN0XXLLXXXXN*
V0023 C01XXXXXXN0XXLLXXXXN*
V0024 C01XXXXXXN0XXLLXXXXN*
V0025 C01XXXXXXN0XXLLXXXXN*
V0026 C01XXXXXXN0XXLLXXXXN*
V0027 C01XXXXXXN0XXLLXXXXN*
V0028 000XXXXXXN1XXZZXXXXN*
V0029 C00XXXXXXN1XXZZXXXXN*
V0030 C00XXXXXXN1XXZZXXXXN*
V0031 C00XXXXXXN1XXZZXXXXN*
V0032 C00XXXXXXN1XXZZXXXXN*
V0033 C00XXXXXXN1XXZZXXXXN*
V0034 C00XXXXXXN1XXZZXXXXN*
V0035 C00XXXXXXN1XXZZXXXXN*
V0036 C00XXXXXXN1XXZZXXXXN*
C1AF6*
~2273
```

In this JEDEC file are the fuse data and so called “vector data” contained. The fuse data describe the programming of the PAL-device. The vector data are only for verifying the programmed PAL on correct work after programming.

From the above JEDEC file the PALASM diassembler creates the following listing:

```
TITLE      2-BIT UP/DOWN COUNTER
PATTERN
REVISION   0.01
AUTHOR     DIRK BECKER, BENG, GROUP A
COMPANY    UEL
DATE       10/07/98, 27/10/98


CHIP  _2BITCNT  PAL16V8

PIN 1 CLK
PIN 2 UP
PIN 3 INIT
PIN 10 GND
PIN 11 OE
PIN 14 R0 REG
PIN 15 R1 REG
PIN 20 VCC


EQUATIONS


     R1  :=  /UP * /INIT * R1 * R0
         +  UP * /INIT * /R1 * R0
         +  UP * /INIT * R1 * /R0
         +  /UP * /INIT * /R1 * /R0
     R0  :=  /INIT * /R0


SIMULATION

     TRACE_ON     INIT  UP  OE  CLK  R0  R1
     SETF     /INIT  /OE  UP  /CLK
     FOR  I  :=  1  TO  4  DO  BEGIN
          CLOCKF     CLK
          CLOCKF     /CLK
     END
     SETF     /INIT  /OE  /UP  /CLK
     FOR  I  :=  1  TO  4  DO  BEGIN
          CLOCKF     CLK
          CLOCKF     /CLK
     END
     SETF     INIT  /OE  /UP  /CLK
     FOR  I  :=  1  TO  4  DO  BEGIN
          CLOCKF     CLK
          CLOCKF     /CLK
     END
     SETF     /INIT  OE  /UP  /CLK
     FOR  I  :=  1  TO  4  DO  BEGIN
          CLOCKF     CLK
          CLOCKF     /CLK
     END
     TRACE_OFF
```

The created PL2 File is without the comments and the original formations because it was automatically generated (diassembled) from the machine coded JEDEC file.

3.7 Use of the AMD programmer ALL07

Last step of the lab was to program the simulated and compiled listing to a real PAL16V8, by use of the AMD programmer ALL07 and the software belonging to it.
With the vector data of the JEDEC file the PAL was verified on correct work.

On the following pages the original Lab printouts are attached.