Lab-Report
ECAD

4-bit multiplier

using Mentor Graphics

Name:	Dirk Becker
Course:	BEng 2
Group:	A
Student No.:	9801351
Date:	08/12/1998

UNIVERSITY of EAST LONDON

1. Contents

2. Introduction

Objectives of the lab was to design a 4-Bit Multiplier using previous created half- and full-adders. A 4-Bit multiplier can be realised by using at least 8 full- and 4 half-adders.
The half-adders can be replaced by full-adders, if one input of the full-adder is grounded.

3. Half-adder design

A Half adder can add 2 different binary digits. So the output can only change between 0, $(01)_2$ or $(10)_2$.
A truth table and the realisation of a half-adder by means of digital circuits is shown at the following figures.

ina	inb	sum	carry
0	**0**	**0**	**0**
0	**1**	**1**	**0**
1	**0**	**1**	**0**
1	**1**	**0**	**1**

figure 2 - truth table

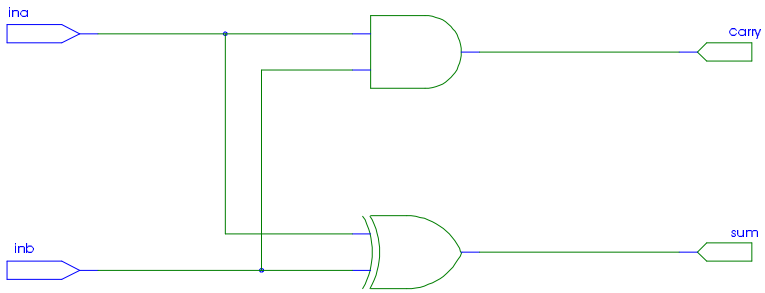

figure 1 - half-adder schematics

The half-adder is realised by means of an And and an Exor latch. The And detects the carry and the Exor the sum of the Inputs ina and inb.
That is realised via the following Boolean-equation:

$$\text{sum} = \text{ina} \cdot \text{inb}$$

$$\text{carry} = \overline{\text{ina}} \cdot \text{inb} + \text{ina} \cdot \overline{\text{inb}}$$

$$\text{carry} = \text{ina} \oplus \text{inb}$$

The different circuits were designed using Graphics and then converted into a Symbol for easier use in the higher level circuits (half-adder → full-adder → multiplier).

4. Full-adder design

Major disadvantage of the half-adder is the capability only to add 2 different digits, whereby mostly the addition of three different digits is necessary. The further development of the half-adder leads to the design of the full adder which is able to add three different binary digits. Mostly a full adder has to add two binary digits and a carry from a previous (full-)adder. Following figures show the truth-table and the schematics of a full-adder.

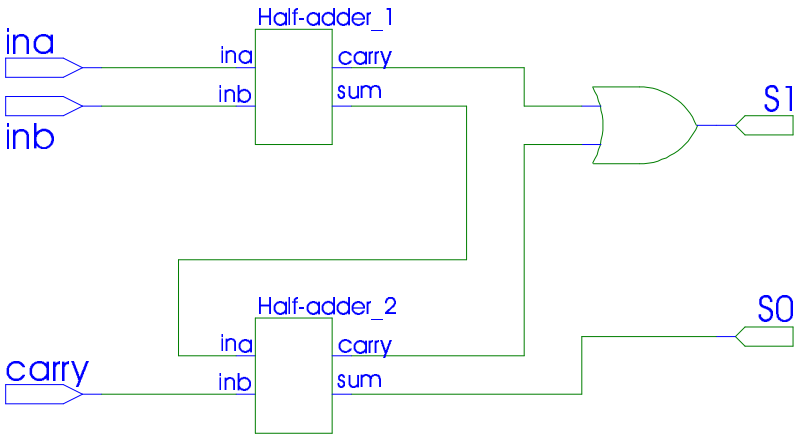

figure 3 - full-adder schematics

carry	inb	ina	S1	S0
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

figure 4 - full-adder truth-table

Boolean-equation for the full-adder:

$$S0 = ina \oplus inb \oplus carry$$

$$S1 = ina \cdot inb + ina \cdot carry + inb \cdot carry$$

5. 4-Bit Multiplier Design

Multiplying binary numbers with digital networks works in the same way like conventional multiplication via shifting and addition.
The following example shows multiplying
$(13)_{10}\cdot(11)_{10}=(143)_{10}\rightarrow(1101)_2\cdot(1011)_2=(10001111)_2$

```
   1101  x  1011

            1101
    +      1101
    +     0000
    +    1101
-------------------
carry:

    +   1111
-------------------
         10001111
```

The following table shows the function of a 4-bit multiplier:

$X_3X_2X_1X_0$ x $Y_3Y_2Y_1Y_0$							
	X_3Y_3	X_2Y_3	X_1Y_3	X_0Y_3			
		X_3Y_2	X_2Y_2	X_1Y_2	X_0Y_2		
			X_3Y_1	X_2Y_1	X_1Y_1	X_0Y_1	
				X_3Y_0	X_2Y_0	X_1Y_0	X_0Y_0
	carry10	carry8	carry4	carry2	carry1		
	carry11	carry9	carry5	carry3	sum2		
		sum10	carry6				
			sum7	sum4			
			sum8	sum5			
carry12= S_7	**sum12= S_6**	**sum11= S_5**	**sum9= S_4**	**sum6= S_3**	**sum3= S_2**	**sum1= S_1**	**S_0**

The borders which contain 2 additions are realised by means of a half-adder (4 at all) and the borders, which contain 3 additions are realised via full-adders (8 at all).
For multiplying two 4-bit binary digits 12 adders are needed.
The realisation of the multiplier using Mentor Graphics is shown on the following pages.
The simulation shows the following multiplication:

```
a) 0000x0000=00000000   (0x0=0) OK
b) 1111x1111=11100001   (15x15=225) OK
c) 0000x1111=00000000   (0x15=0) OK
d) 0101x0101=00011001   (5x5=25) OK
e) 0011x0011=00001001   (3x3=9) OK
```

There are also Printouts of the half- and the full-adder using Mentor Graphics.